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Dyplo® for (aero)space applications

Introduction

Dyplo is a tool set, an IP infrastructure on the FPGA and a software library that significantly simplifies the dynamic partial reuse and programming of FPGA logic.

The interface provided by Dyplo makes is easy and transparent for software application developers to program, execute and change functionality in the FPGA. Changing or replacing the functionality can be done at run time on the fly, without disturbing other functionality in the FPGA. Dyplo enables software developers to easily deploy functionality, written in C/C++, on the FPGA without the help of VHDL engineers. This gives software developers a new way of accelerating algorithms and minimizing power consumption. VHDL engineers also benefit from using Dyplo. They can easily connect their VHDL-programmed-logic and IP cores to the configurable Dyplo network-on-chip (NOC) framework, which will then take care of the interfacing with software and the other FPGA deployed functionality.

Dyplo also helps to speed up application development effort itself by significantly reducing the waiting-time between changing source code (VHDL or C/C++) and testing it on the FPGA itself. This is a direct result of the fact that Dyplo partitions the FPGA in multiple reusable areas that are synthesized and place and routed independently.

Dyplo does this all by exploring the capabilities of a partial reconfiguration feature that is present in modern SRAM-based-FPGAS.

Topic – ESA collaboration

ESA and Topic Products consider partial reconfiguration very useful for space applications for a number of reasons: It enables reuse of the same hardware for different functions at different times. It also helps in mitigating single event upsets, since functionality can easily be reprogrammed partially, without interrupting unaffected functionality. It enables more reliable upgrading of functionality (even remotely) and allows for a simpler way to save power by removing functionality from the FPGA when it is not needed.

However, until now, partial reconfiguration is not used very often in applications, as it is considered very difficult. Dyplo changes this by taking care of these complicating aspects. Therefore, ESA and Topic Products have teamed up to enhance the Dyplo infrastructure to make it qualified for space applications. A three-step approach is taken to make Dyplo suitable for space applications:

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1. System integration

Dyplo is made compatible with the radiation hardened Xilinx Virtex 5QV FPGA technology in combination with the RTEMS real-time operating system on a fault tolerant LEON softcore processor. The Dyplo software driver and API are mapped on the RTEMS OS and to the Dyplo HDL IP block is ported to Virtex 5 FPGA technology and the Xilinx development tool-set. The design flow management tool (Dyplo Development Environment) remains the same and compatible with a non-space qualified version.

2. Robustness for SEU's

The Dyplo FPGA NOC infrastructure itself is enhanced to make it more robust for SEU's. SEU mitigation components are provided to help application developers to mitigate SEU effects in their algorithms.

3. Space qualified hardware

Additional effort is spend to make non-space qualified hardware reliably available for space missions by using Dyplo. This is realized in conjunction with the qualification of Topic's System-on-Modules for space. These System-on-Modules for a family of processing platforms (www.topic.nl). The benefits of using pre-qualified boards are the reduction of board design costs, the simplification of the qualification process as well as the certification effort. The combination of Dyplo with the space qualified hardware delivers a powerful processing platform with in-flight partial reconfiguration and selective capabilities for remote updates and upgrades.

Technical impact

Dyplo makes extensive use of partial reconfiguration of SRAM based FPGA devices. This is realized by creating a configurable Network-on-Chip infrastructure on the FPGA around fixed and reconfigurable partitions and third-party IP cores. The Dyplo infrastructure takes care of streaming data between partitions. This gives operating system like properties to FPGA executed processes like treading, data streaming, synchronization, etc. Especially the partial reconfigurable areas give the FPGA special capabilities in combination with runtime configuration and validation of the programmed functionality.

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